Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) An apparatus for generating PN (pseudo noise) codes comprising:

a control unit for outputting a control signal for ~~the~~ a normal state or a PN chip advance;

a plurality ~~MUXs~~ of multiplexers for outputting an output value of ~~the~~ a next state for a normal operation or an output value of a following next state ($\vec{r}_{m+2}$) for a PN chip advance as an output signal in response to the control signal of said control unit;

a plurality of shift registers ~~connected~~ for outputting a PN chip ~~codes~~ code of ~~the~~ a next state ($\vec{r}_{m+1}$) or ~~the second~~ a following next state ($\vec{r}_{m+2}$) during one system clock time period in response to said outputs of the multiplexers ~~MUXs~~, ~~the~~ an input ~~end~~ of each of said shift registers being connected to ~~the~~ an output end of each of said ~~MUXs~~ multiplexers,

wherein to obtain the output value of the following next state ($\vec{r}_{m+2}$) of shifter registers for one PN chip advance, the output values are determined based on the following equation:

$$\vec{r}_{m+2} = \lfloor r_{n,m+2}\ r_{n-1,m+2}\ \cdots\cdots\ r_{1,m+2}\ 0 \rfloor$$

$$r_{i,m+2} = \begin{cases} r_{i-2,m} \oplus (r_{n,m} g_{i-2}) \oplus \left[\{r_{n-1,m} \oplus (r_{n,m} g_{n-1})\} g_{i-1}\right], & 1 < i \le n, \text{wherein } i \text{ is an integer} \\ r_{n-1,m} \oplus (r_{n,m} g_{n-1}) & , i = 1 \\ 0 & , i = 0 \end{cases}$$

wherein $\vec{r}_m$ is present state values of the shifter registers and $\vec{g}_n$ is parameter values of a generation polynomial.

2. (Currently Amended) The apparatus for generating PN codes according to claim 1, wherein said control unit further outputs a control signal for ~~a~~ one PN chip retard; and wherein said ~~MUXs~~ multiplexers further ~~outputs~~ ~~a~~ output an output value of the retard state for ~~said~~ one PN chip retard.

3. (Currently Amended) A method ~~for~~ of generating PN codes in ~~an n stage~~ a PN code generator comprising ~~an LSSR (linear sequence shift register) including a number of shift registers connected in series and n number of MUXs, the output end of each of the n number of MUXs being connected to input end of said n shift registers, said method comprising the steps of~~ shift registers and using an nth order generation polynomial g(X)

$$g(X) = g_n X^n + g_{n-1} X^{n-1} + \cdots\cdots + g_1 X + 1 \ ,$$

the method comprising:

determining parameter values ($\vec{g}_n$) of the nth order generation polynomial by a first equation, wherein the first equation is

$$\vec{g} = [g_n g_{n-1} \quad \cdots\cdots \quad g_1 g_0] \ ,$$

$$g_i = \begin{cases} 1 & , i = n \\ 0 \text{ or } 1 & , 0 < i < n, \quad \text{wherein i is an interger} \\ 1 & , i = n \end{cases} ;$$

determining present states ($\vec{r}_m$) of shift registers of the PN code generator by a second equation, wherein the second equation is

$$\vec{r}_m = [r_{n,m} \quad r_{n-1,m} \quad \cdots\cdots r_{1,m} \quad r_{0,m}]$$

$$r_{i,m} = \begin{cases} 0 \text{ or } 1 & , 0 < i \le n, \quad \text{wherein i is an interger} \\ 0 & , i = 0 \end{cases} ; \text{ and}$$

inputting state values into the sift registers for providing advanced states ($\vec{r}_{m+2}$) of the shift registers based on a third equation using the present states ($\vec{r}_m$) of the shift registers and the parameter values ($\vec{g}_n$), wherein the third equation is

$$\vec{r}_{m+2} = [r_{n,m+2} \ r_{n-1,m+2} \cdots\cdots r_{1,m+2} \ 0] .$$

$$r_{i,m+2} = \begin{cases} r_{i-2,m} \oplus (r_{n,m} g_{i-2}) \oplus \left[\{r_{n-1,m} \oplus (r_{n,m} g_{n-1})\} g_{i-1}\right], & 1 < i \le n, \text{wherein } i \text{ is an integer} \\ r_{n-1,m} \oplus (r_{n,m} g_{n-1}) & , i = 1 \\ 0 & , i = 0 \end{cases}$$

~~inputting signals to perform an operation for obtaining the next state of the LSSR in the normal state and an operation for obtaining the next state of the LSSR for a PN chip advance into each of the n MUXs;~~

~~generating the control signals for changing the next state in respect to the LSSR;~~

~~multiplying signals input to each of the MUXs in response to the control signals; and~~

~~performing an operation corresponding to the multiplied signals during one clock.~~

4. (Currently Amended) The method for generating PN codes according to claim 3, wherein ~~said operation for obtaining the next state of the LSSR for the PN chip advance~~ further ~~comprises~~: the PN generator uses a same system clock as on output rate of the PN generator

~~inputting a resultant value of OR operating an output signal of (n-1)th shift register and a resultant value of AND operating an output signal of nth shift register and (n-1)th value of generation polynomial given to the PN code generator into an input end of first shift register of the n number of shift registers; and~~

~~inputting a resultant value of OR operating first, second and third values at the same time into the input end of random ith shift register except the first shift register, the first value being obtained from OR operating an output signal of (i-1)th shift register of generation polynomial and a resultant value of OR operating an output signal of the (n-1)th shift register and a resultant value of AND operating an output signal of the nth shift register and the (n-1)th value of the generation polynomial, the second value being obtained from AND operating an output signal of the nth shift register and (i-2)th value of the generation polynomial, and the third value being an output signal of an (i-2)th retard device~~.

5. (Currently Amended) The method for generating PN codes according to claim 3, ~~wherein~~ further comprising:

performing an operation for ~~the~~ a PN chip retard for the LSSR ~~is performed to disable~~ by disabling external enable signals applied to each of the shift registers during one PN chip time period.

6-16. (Canceled).

17. (New) A method of generating a PN code in a PN code generator comprising N number of shifter registers and using a same system clock as a PN chip rate, the method comprising:

calculating advanced state values of each shift register based on present state

values of each shifter register; and

generating the PN code according to the advanced state values during one system clock time.

18. (New) The method of claim 17, wherein the advanced state value is calculated based on the present state value using the following equation:

$$\vec{r}_{m+2} = \lfloor r_{n,m+2} r_{n-1,m+2} \cdots\cdots r_{1,m+2}\ 0 \rfloor$$

$$r_{i,m+2} = \begin{cases} r_{i-2,m} \oplus (r_{n,m} g_{i-2}) \oplus \left[\{r_{n-1,m} \oplus (r_{n,m} g_{n-1})\} g_{i-1}\right], & 1 < i \le n, \textit{wherein } i \textit{ is an integer} \\ r_{n-1,m} \oplus (r_{n,m} g_{n-1}) & , i = 1 \\ 0 & , i = 0 \end{cases}$$

wherein $\vec{r}_{m+2}$ is the advanced state values of an nth shifter registers and $\vec{r}_m$ is the present state values of the shifter registers.